Remarks/Arguments:

Claims 1-16 and 18-24 are pending in the above-identified application. Claims 3 and 17 are cancelled.

Claims 1, 2, 4, 6-7, 12, 15 and 22 were rejected under 35 U.S.C. § 112, first paragraph. In particular, the Examiner asserts that the term "predetermine range" is not supported in the specification. The claims have been amended to amend the claims to recite "predetermined value."

Claim 1 is amended to include,

> ... applying a first test stress to selected cells of the plurality of memory cells with a built-in self test by performing a plurality of test sequences, wherein each of said test sequences includes a test pattern used with a plurality of conditions and **the plurality of conditions are different between each of said test sequences** (Emphasis added).

Basis for these amendments may be found in the specification at page 9, lines 7-21 and Figure 1. With regard to claim 1, Giles et al. does not disclose or suggest applying a first test stress using a plurality of different conditions with a test pattern. Giles et al. conducts a first test by setting a first environmental condition used with a predetermined pattern. (Col. 8, lines 5-24). Then, after the first test is completed, a repair cycle is made at block 72. Next, Giles et al. conducts a second test by setting a second environmental condition used with a predetermined pattern. (Col. 8, lines 37-39). Then, after the second test is completed, a second repair cycle is made at block 80. Thus, Giles et al. applies only one condition to a pattern for each test. That is, Giles et al. applies only one condition to a pattern prior to each repair cycle being run. In contrast, as described in the exemplary embodiment at page 9 of Applicants' invention, for each test and before repairs are made "different test patterns and/or different conditions may be selected." Applicant's claimed feature of applying a first test stress using a plurality of different conditions with a test pattern is advantageous over the prior art because more weak cells can be repaired using less repair cycles. Thus, claim1 is allowable over the art of record.

Claims 7 and 12, while not identical to claim 1 include features similar to those set forth above with regard to claim 1. Thus, claims 7 and 12 are also allowable over the art of record for reasons similar to those set forth above with regard to claim 1.

Claims 21-24 were rejected under 35 U.S.C. § 102 (b) as being anticipated by Giles et al. Claims 21-22 depend from claim 1. Claim 23 depends from claim 7. Accordingly, claims 21-23 are not subject to rejection under 35 U.S.C. § 102(b) in view of Giles et al.

Claim 15, as amended, includes features neither disclosed nor suggested by the cited art, namely:

> ...a first delay circuit comprising...
>
> ...a first timer for applying a plurality of timings to the memory cells, the plurality of timings including an operational timing mode within a predetermined timing range, a plurality of relaxed timing modes that exceeds the predetermined timing range and a plurality of tightened timing modes that is less than the predetermined timing range...
>
> ...a second timer for modifying at least one of the plurality of timings...
>
> ...a second delay circuit coupled to the first delay circuit for modifying at least one of the plurality of timings to provide a timing that exceeds the plurality of relaxed timing modes...

These features are disclosed, for example, p. 11, lines 5-12; p. 11, line 20; p. 12, line 7 and Figs. 2-5.

Templeton et al. disclose, in Figs. 3 and 4, providing a stress clock signal 304 to perform a high stress BISR on an ASIC memory during power up or global reset of the ASIC or an internal clock signal 302 during normal operation of the memory array (Col. 7, lines 52-63). As shown in Fig. 4 of Templeton et al., a memory clock generator 402 provides an internal clock signal 302 and stress clock signal 304 to multiplexer 408 (Col. 8, line 66-Col. 9, line 3). Templeton et al. do not disclose or suggest Applicants claimed features of "...a first delay circuit comprising... a first timer for applying a plurality of timings... including... a plurality of relaxed timing modes that exceeds the predetermined timing range" or "a second delay circuit coupled to the first delay circuit... to provide a timing that exceeds the plurality of relaxed timing modes... (emphasis added). These features are neither disclosed nor suggested by Templeton et al.

In view of the foregoing amendments and remarks, this Application is in condition for allowance which action is respectfully requested.

Respectfully submitted,

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The Director is hereby authorized to charge or credit Deposit Account No. **18-0350** for any additional fees, or any underpayment or credit for overpayment in connection herewith.

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